AMENDMENTS TO THE CLAIMS

Amended claims follow:

1. (Currently Amended) An integrated circuit, comprising:

an active circuit;

a metal layer disposed, at least partially, above the active circuit; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer is meshed;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process;

wherein the bond pad is only disposed above an outer periphery of an input/output (I/O) bus of the active circuit;

wherein an interconnect metal layer of the metal layer is electrically coupled to a plurality of underlying metal layers by way of vias, the plurality of underlying metal layers disposed at least in part below the active circuit;

wherein the interconnect metal layer interconnects the bond pad with the plurality of underlying metal layers;

wherein the interconnect metal layer of the metal layer is meshed by including a plurality of openings, the openings defining a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect, where interconnect vias formed in rows along a length of at least the first portions provide communication between the interconnect metal layer and the bond pad;

wherein the openings are adapted for facilitating an interlock between the interconnect metal layer of the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

2.-5. (Cancelled).

6. (Currently Amended) The integrated circuit as recited in claim [[5]]1, wherein each of the underlying metal layers is in electrical communication by way of ~~a plurality of~~the vias.

7. (Cancelled)

8. (Cancelled)

9. (Currently Amended) The integrated circuit as recited in claim [[8]]1, wherein the inter-metal dielectric layer is constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material.

10. (Currently Amended) The integrated circuit as recited in claim [[7]]1, wherein the openings are completely enclosed around a periphery thereof.

11. (Currently Amended) The integrated circuit as recited in claim [[7]]1, wherein the openings have a substantially square configuration.

12. (Cancelled)

13. (Currently Amended) The integrated circuit as recited in claim [[12]]1, wherein the openings define a matrix of openings.

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) The integrated circuit as recited in claim 1[[5]], wherein the interconnect vias include one single row for each of the first portions.

17. (Currently Amended) The integrated circuit as recited in claim 1[[5]], wherein the interconnect vias include at least two spaced rows for each of the first portions.

18. (Original) The integrated circuit as recited in claim 17, wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions.

19. (Cancelled)

20. (Currently Amended) An integrated circuit, comprising:

an active circuit means for processing electrical signals;

a metal layer disposed, at least partially, above the active circuit means and including a mesh means for preventing damage incurred during a bonding process; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit means;

wherein the mesh means ensures that bonds are capable of being placed over the active circuit means without damage thereto during a bonding process;

wherein the active circuit means includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh means ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process;

<u>wherein the bond pad is only disposed above an outer periphery of an input/output (I/O) bus of the active circuit means;</u>

wherein an interconnect metal layer of the metal layer is electrically coupled to a plurality of underlying metal layers by way of vias, the plurality of underlying metal layers disposed at least in part below the active circuit means;

wherein the interconnect metal layer interconnects the bond pad with the plurality of underlying metal layers;

wherein the interconnect metal layer of the metal layer is meshed by including a plurality of openings, the openings defining a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect, where interconnect vias formed in rows along a length of at least the first portions provide communication between the interconnect metal layer and the bond pad;

wherein the openings are adapted for facilitating an interlock between the interconnect metal layer of the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

21. (Currently Amended) An integrated circuit, comprising:

a semiconductor structure including an active circuit including an input/output (I/O) bus and a plurality of transistors forming a core of circuits;

a plurality of vertically spaced underlying metal layers disposed, at least partially, under the active circuit and around a periphery thereof, wherein each of the underlying metal layers are in electrical communication by way of a plurality of underlying vias with the active circuit and other underlying metal layers;

a meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit and around a periphery thereof, the interconnect metal layer being in electrical communication with the underlying metal layers by way of a plurality of additional vias;

an inter-metal dielectric layer disposed, at least partially, above the interconnect metal layer, the inter-metal dielectric layer constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material;

a top metal layer disposed, at least partially, above the inter-metal dielectric layer, the top metal layer for serving as a bond pad, the top metal layer being in electrical communication with the interconnect metal layer by way of a plurality of interconnect vias; and

a passivation layer disposed, at least partially, above the top metal layer.

wherein the interconnect metal layer is meshed for preventing damage incurred during a bonding process;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during the bonding process;

wherein an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process;

wherein the bond pad is only disposed above an outer periphery of the I/O bus of the active circuit;

wherein the interconnect metal layer is electrically coupled to the plurality of underlying metal layers by way of vias;

wherein the interconnect metal layer interconnects the bond pad with the plurality of underlying metal layers;

wherein the interconnect metal layer is meshed by including a plurality of openings, the openings defining a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect, where the interconnect vias are formed in rows along a length of at least the first portions and provide communication between the interconnect metal layer and the bond pad;

wherein the openings are adapted for facilitating an interlock between the interconnect metal layer of the metal layer and the inter-metal dielectric layer disposed between the metal layer and the bond pad.

22. - 26. (Cancelled)

27. (Previously Presented) The integrated circuit as recited in claim 1, wherein the metal layer is disposed, at least partially, above the active circuit along a vertical axis.

28. (Cancelled)

29. (Currently Amended) The integrated circuit as recited in claim [[8]]1, wherein the inter-metal dielectric layer is constructed from a low-K dielectric material.

30. (Currently Amended) The integrated circuit as recited in claim [[8]]1, wherein the inter-metal dielectric layer is constructed from a fluorinated silica glass (FSG) material.

31. (Cancelled)